IPW

PATENTS
Docket No. LT-170

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Daniel Eddleman

Application No.: 10/761,501 Confirmation No.: 4096

Filed : January 20, 2004

For : METHODS AND CIRCUITS FOR TRACKING AND SEQUENCING MULTIPLE POWER SUPPLIES

Group Art Unit : 2838

Mail Stop Amendment
Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR
INFORMATION DISCLOSURE STATEMENT

Sir:

Transmitted herewith is an Information Disclosure Statement in the above-identified application. This Statement is submitted:

[ ] within three months of the application filing date;

[X] more than three months from the application filing date but before the mailing date of the first Office Action on the merits.

In accordance with 37 C.F.R. § 1.97, submission of this Statement requires no fee. However, if for any reason a fee is due, the Director is hereby authorized to charge payment of any fees required in connection with this Information Disclosure Statement to Deposit Account

No. 06-1075. A duplicate copy of this letter is transmitted herewith.

Respectfully submitted,

Chi Hsin Chang

Chi-Hsin Chang
Registration No. 52,717
Agent for Applicant

FISH & NEAVE LLP
Customer No. 1473
1251 Avenue of the Americas
New York, New York 10020-1104
Tel.: (650) 617-4000

I hereby Certify that this Correspondence is being Deposited with the U.S. Postal Service as First Class Mail in an Envelope Addressed to : HON. COMMISSIONER FOR PATENTS, P.O. BOX 1450, Alexandria, VA 22313-1450 on:

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INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, applicant hereby makes the following documents of record in the above identified application:*

* Applicant's submission of this statement is not an admission that the information herein is, or is considered to be, material to patentability of any presented claim. With respect to cited documents other than patents, Applicant has identified dates or possible date codes that appear on the documents. Applicant's identification of these dates is not an admission that the documents were published by or on the dates identified. Applicant reserves the right to challenge the status of any of the cited documents and information as prior art.

Other Documents

Galinski, Martin; "Circuit manages power-up sequencing"; EDN; October 31, 2002.

Linear Technology; "LT1645 Dual-Channel Hot Swap Controller/Power Sequencer"; Datasheet; 1999.

Linear Technology; "LTC2920-1/LTC2920-2 Single/Dual Power Supply Margining Controller"; Datasheet, Initial Release; March 2003.

Linear Technology; "LTC3205 Multidisplay LED Controller"; Datasheet, Initial Release; August 2003.

Maxim Integrated Products; "MAX5039/MAX5040 Voltage-Tracking Controllers for PowerPC, DSPs, and ASICs"; Datasheet; May 2002.

Summit Microelectronics, Inc.; "SMT4004 QUAD TRAKKING™ POWER SUPPLY MANAGER", Datasheet; June 9, 2003.

Summit Microelectronics, Inc.; "SMT4004 QUAD TRACKING POWER SUPPLY MANAGER ADVANCED CURRENT SENSING SCHEMES AND POWER MOSFET SELECTION"; Application Note 20; February 21, 2002.

Summit Microelectronics, Inc.; "SMT4004 QUAD TRACKING POWER SUPPLY MANAGER Windows GUI Users Guide and Configuration Register Descriptions"; Application Note 22; August 23, 2002.

Summit Microelectronics, Inc.; "SMT4004-Advanced Voltage Tracking Methods Boost Efficiency, Reliability"; Application Note 26, Advance Information; October 16, 2002.

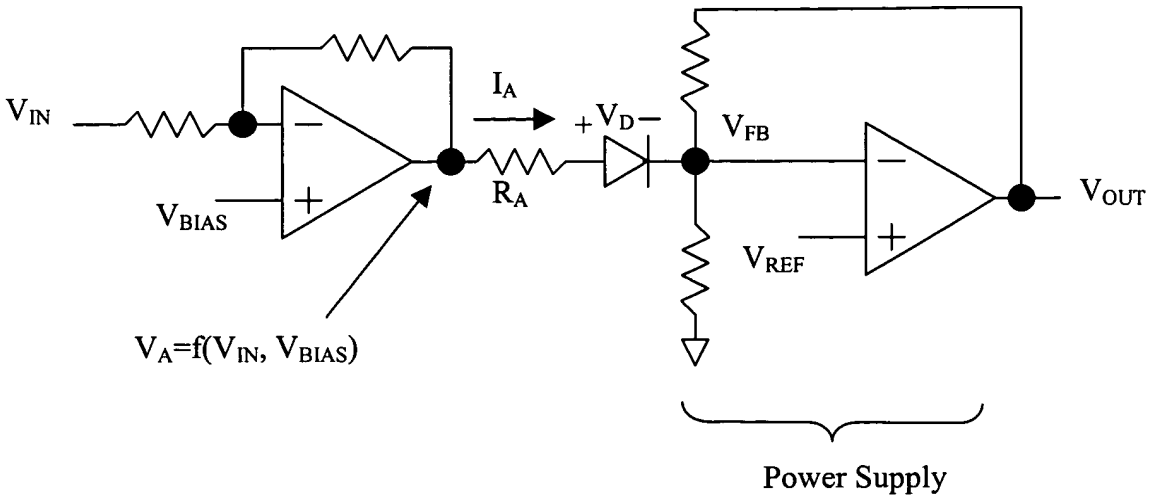
Summit Microelectronics, Inc.; "Xilinx Virtex™-E, Spartan™-IIE FPGA and SMT4004 TRAKKER™ Supply Manager Reference Design: Procedure and Results Summary"; Application Note 31; January 7, 2003.

Summit Microelectronics, Inc.; "Lossless Tracking Procedure and Results Summary Reference Design: Xilinx Virtex™-E, Spartan™-IIE FPGA and SMT4004 TRAKKER™"; Application Note 34; January 7, 2003.

Other Information

The following are two previously-known techniques that can be used to generate a signal that is injected into the feedback network. Applicant respectfully submits that the inventions claimed in the present application are patentable over the following two techniques.

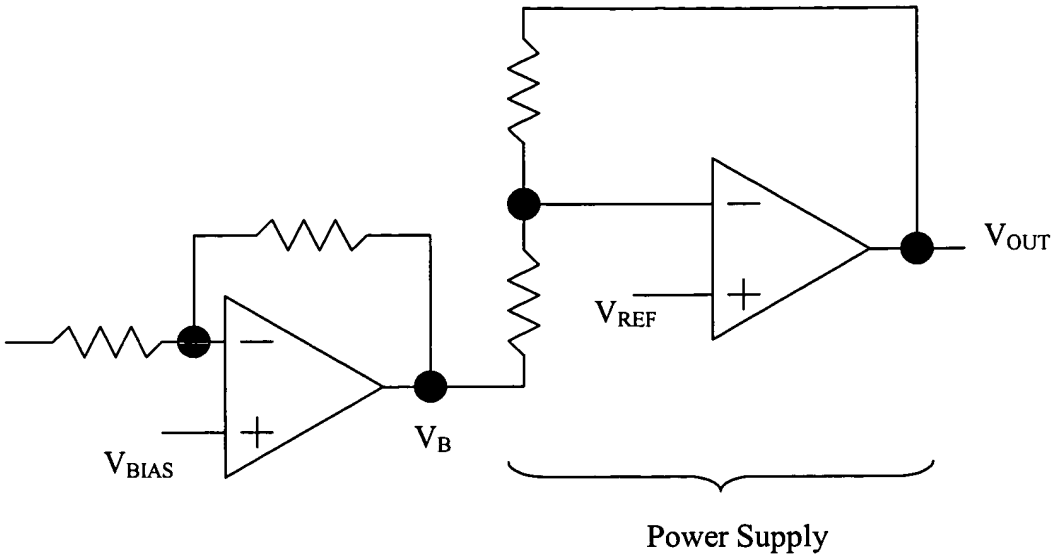
(1) A resistor could be connected between a voltage source and the feedback node to adjust the output voltage.



$$I_A = \frac{V_A - V_{FB} - V_D}{R_A} \approx \frac{V_A - V_{FB}}{R_A}$$ when the diode is forward biased.

While ramping, this presents a different impedance at the feedback node, which could affect stability.

(2) A voltage could be forced at the bottom of a resistor coupled to the feedback node, which effectively injects a signal into the feedback node.

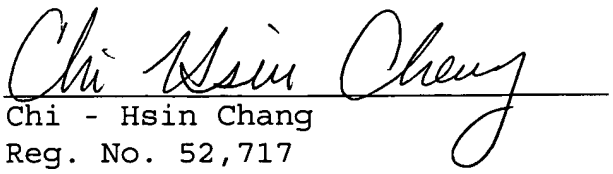


V_B alters the current through the feedback resistors. There is an error voltage after the supply has completely ramped-up due to the non-zero V_B voltage. Also, the op-amp's feedback loop may interact with the power supply's feedback loop.

It is respectfully requested that these documents be (1) fully considered by the Patent and Trademark Office during the examination of this application; and (2) printed on any patent that may issue on this application. Applicant requests that a copy of Form PTO-1449, as considered and initialed by the Examiner, be returned with the next communication.

An early and favorable action is respectfully requested.

Respectfully submitted,



Chi - Hsin Chang
Reg. No. 52,717
Agent for Applicant

Mark D. Rowland
Reg. No. 32,077
Attorney for Applicant

FISH & NEAVE LLP
Customer No. 1473
1251 Avenue of the Americas
New York, New York 10020-1104
Tel.: (650) 617-4000

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Lorraine Coke
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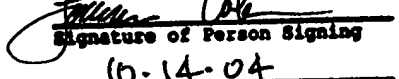
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Date of Signature

FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. **LT-170**	SERIAL NO. **10/761,501**
	INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANT **Daniel Eddleman**	
		FILING DATE **January 20, 2004**	GROUP **2838**

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIALS	
	Galinski, Martin; "Circuit manages power-up sequencing"; EDN; October 31, 2002.
	Linear Technology; "LT1645 Dual-Channel Hot Swap Controller/Power Sequencer"; Datasheet; 1999.
	Linear Technology; "LTC2920-1/LTC2920-2 Single/Dual Power Supply Margining Controller"; Datasheet, Initial Release; March 2003.
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EXAMINER DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.